REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 3 and 5 were previously cancelled. Claims 1, 2, 4 and 6-20 are pending in the application.

I. Rejection under 35 U.S.C. § 103

In the Office Action, at page 2, claims 1, 4, 6-8, 11, 12, 14, 15 and 17-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,446,213 to Yamaki in view of U.S. Patent No. 6,336,161 to Watts.

In the Office Action, at page 2, claims 1, 2, 6, 9, 10, 13, 14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaki in view of U.S. Patent No. 2003/0145191 to Park.

These rejections are respectfully traversed because Yamaki in view of Watts or Park does not suggest:

> a controller to enable a power saving standby mode, to control the power management controller to store an operating state stored in the system memory to the flash memory, and to cut power supply to the system when the power saving standby mode is selected,

as recited in independent claim 1.

Further, Yamaki in view of Watts or Park does not discuss or suggest:

> selecting a power saving standby mode;
>
> storing an operating state stored in the system memory to a flash memory when the power saving standby mode is selected; and
>
> cutting power supply to the system after the operating state has been stored,

as recited in independent claim 6.

In addition, Yamaki in view of Watts or Park does not discuss or suggest:

> a controller to control the power management controller to store an operating state data stored in the system memory to the flash memory when a power saving standby mode is selected, to cut the power supply to the system, and to store the operating state to the system memory when a normal mode is selected,

as recited in independent claim 14.

Also, Yamaki in view of Watts or Park does not discuss or suggest:

> copying an operating state data stored in the system memory to a flash memory when a power saving standby mode of the computer system is activated; and
>
> copying the operating state data back to the system memory when a normal mode of the computer system is activated,

as recited in independent claim 18.

Further, Yamaki in view of Watts or Park does not discuss or suggest:

> a basic input/output system of the computer system storing an operating state stored in the system memory to the flash memory and cutting power supply to the system, after being informed that the power saving standby mode is selected,

as recited in independent claim 20.

As a non-limiting example, the present invention as set forth in claim 1, for example, is directed to a computer system that includes a system memory, a power management controller, a flash memory, and a controller. The controller enables a power saving standby mode and controls the power management controller to store an operating state stored in the system memory to the flash memory and to cut power supply to the system when the power saving standby mode is selected.

Yamaki discusses a software-based sleep control of an operating system in which, when a power supply switch is depressed while the computer system remains in a sleep state of a soft-off state, a wakeup event is generated in an embedded controller 18. In Yamaki, state S3 is a sleep state in which there is no need to hold the preset hardware environment values, though the value preset for the main memory must be held, which means that the devices are set into this sleep mode when the power supply switch of the system is turned off (D3). The hardware environment context is saved in the main memory.

However, because the system memory is a volatile memory, standby power needs to be continually supplied to save the hardware environment values stored in the system memory of Yamaki. Yamaki does not, therefore, discuss or suggest that the embedded controller 18 controls the power supply controller 15 to store an operating state stored in the system memory to a flash memory and to cut power supply to the system when the power saving standby mode is selected. Yamaki requires that standby power is supplied to the system as the operating state is stored in the system in order to save operating state data. As the Examiner concedes, Yamaki does not teach storing the operating state to a flash memory and cutting off the power.

The Examiner alleges that Watts and Park make up for the deficiency in Yamaki. The Applicant respectfully disagrees.

Watts discusses that after a power-down mode is initiated, hardware configuration information is stored in the flash EEPROM and once all system information has been stored to either the flash EEPROM or the hard drive, the computer 10 is powered down.

Park discusses a computer system in which, when the computer system comes into a power saving mode 32, if a system memory card is connected to the computer system, last operation data is stored in the system memory card 36.

Neither Watts nor Park discuss or suggest enabling a power saving standby mode and additionally storing the system memory to the flash memory and cutting the power supply to the system, as recited in claim 1, for example. The Examiner alleges that it would have been obvious to one of ordinary skill in the art to combine the teachings of Yamaki with Watts because both Watts and Yamaki are directed toward systems and method of power management for computers. The Examiner further alleges that:

> Watts teaches that power is completely removed from the system [col. 4, lines 66-67] instead of being maintained in a sleep mode...[and that] [s]ince power is completely removed from the system, a greater power saving is achieved over a sleep mode. Additionally, Watts teaches that storing the operating state to a flash memory allows for quick return to the previous operating state [col. 2, lines 38-49].

However, the motivation must be enough to suggest combining the teachings of Yamaki and Watts to one of ordinary skill in the art. While Watts does discuss that the prior operation state of the computer system can be quickly restored upon power-up, the Examiner provides no motivation for specifically combining enabling a power saving standby mode and storing an operating state to the flash memory and cutting power supply to the system.

First, the motivation to combine the references that "since power is completely removed from the system, a greater power saving is achieved over a sleep mode" does not come from the prior art, but comes from the present specification. Particularly, the present specification recites that "it is an aspect of the present invention to provide a computer system according to which a time required to enter a standby mode and return to a normal mode and power consumption required during the standby mode is sharply reduced." Thus, the motivation cited by the Examiner comes not from the prior art, as the Watts reference does not specify that the greater power saving is achieved over a sleep mode. Watts merely recites that since returning to a prior state is simplified, the computer system may be powered down more often, resulting in vastly

improved power use, but Watts does not discuss that a greater power saving is achieved over a sleep mode since power is completely removed from the system. M.P.E.P. § 2142 recites that "[t]he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The motivation cited comes not from the prior art, but is based on the applicant's disclosure.

Further, the motivation cited does not suggest why it would have been obvious to combine the teachings of Yamaki with respect to the power saving standby mode with the teachings of Watts with respect to cutting the power supply to suggest enabling a power saving standby mode and additionally storing an operating state to flash memory and cutting the power supply to the system. Specifically, the power saving standby mode does not require the computer to go through a normal booting process, thus allowing the system to be operated more quickly than when powered down completely. The motivation provided that "a greater power saving is achieved over a sleep mode" does not suggest why one of ordinary skill in the art would specifically utilize the power saving standby mode with the teachings of Watts. Merely reciting that greater power saving is achieved is not an adequate motivation to suggest combining Yamaki and Watts to one of ordinary skill in the art.

In addition, the motivation cited that "storing the operating state to a flash memory allows for a quick return to the previous operating state" is a motivation found in Watts, and the motivation does not suggest why one of ordinary skill in the art would be inclined to combine the power saving standby mode, which does not require the computer to go through a normal booting process, with the teachings of Watts, without having to rely on the applicant's own disclosure to suggest such.

Therefore, the combination of the teachings of Yamaki and Watts does not suggest "a controller to enable a power saving standby mode, to control the power management controller to store an operating state stored in the system memory to the flash memory, and to cut power supply to the system when the power saving standby mode is selected," as recited in independent claim 1, does not discuss or suggest "selecting a power saving standby mode; storing an operating state stored in the system memory to a flash memory when the power saving standby mode is selected; and cutting power supply to the system after the operating state has been stored," as recited in independent claim 6, does not discuss or suggest "a controller to control the power management controller to store an operating state data stored in the system memory to the flash memory when a power saving standby mode is selected, to cut

the power supply to the system, and to store the operating state to the system memory when a normal mode is selected," as recited in independent claim 14, and does not discuss or suggest "copying an operating state data stored in the system memory to a flash memory when a power saving standby mode of the computer system is activated; and copying the operating state data back to the system memory when a normal mode of the computer system is activated," as recited in independent claim 18, and does not suggest "storing an operating state stored in the system memory to the flash memory and cutting power supply to the system, after being informed that the power saving standby mode is selected," as recited in independent claim 20, claims 1, 6, 14, 18 and 20 patentably distinguish over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

As to Park, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to combine the teachings of Yamaki with Park because both Yamaki and Park provide methods for saving the operating state of the computer prior to switching to a lower power mode. The Examiner further alleges that:

> The flash memory of Park provides a number of advantages, including portability, and facilitating increased power saving by completely removing power from the system [paragraph 9]...[and] the teachings of Park would improve the system of Yamaki by providing these features.

However, the motivation cited here is not enough to suggest combining the teachings of Yamaki and Park to one of ordinary skill in the art. Specifically, the Examiner provides no motivation for specifically combining enabling a power saving standby mode and storing an operating state to the flash memory and cutting power supply to the system. The Examiner merely presents a motivation for storing an operating state to the flash memory, but does not suggest why one of ordinary skill in the art would be inclined to combine the power saving standby mode of Yamaki with the storage to flash memory of Park.

Additionally, the Examiner has provided no motivation to suggest combining a power saving standby mode of Yamaki with cutting power to the system as in Park. The motivation cited merely suggests why one of ordinary skill would be motivated to use flash memory or cut power from the system, but does not suggest why one of ordinary skill in the art would be motivated to save to flash memory and cut power to the system when a power saving standby mode is used, the power saving standby mode being different from the powered down mode in that the power saving standby mode does not go through a normal booting process so that the system can be operated quickly.

Further, the motivation provided does not come from Park, but is based on the applicant's own disclosure. The Examiner alleges that paragraph 0009 discusses that Park facilitates increased power saving by completely removing power from the system, but paragraph 0009 does not include a discussion of increasing power saving by completely removing power from the system.

Therefore, as Park does not discuss or suggest "a controller to enable a power saving standby mode, to control the power management controller to store an operating state stored in the system memory to the flash memory, and to cut power supply to the system when the power saving standby mode is selected," as recited in independent claim 1, Park does not discuss or suggest "selecting a power saving standby mode; storing an operating state stored in the system memory to a flash memory when the power saving standby mode is selected; and cutting power supply to the system after the operating state has been stored," as recited in independent claim 6, and does not discuss or suggest "a controller to control the power management controller to store an operating state data stored in the system memory to the flash memory when a power saving standby mode is selected, to cut the power supply to the system, and to store the operating state to the system memory when a normal mode is selected," as recited in independent claim 14, claims 1, 6 and 14 patentably distinguish over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 2, 7-13, 15-17 and 19 depend either directly or indirectly from independent claims 1, 6, 14 and 18 and include all the features of their respective independent claims, plus additional features that are not discussed or suggested by the reference relied upon. For example, claim 13 recites that "the controller controls the power management controller to copy the operating state stored in the flash memory to the system memory via the universal serial bus port when the power saving mode is changed to a normal mode." Therefore, claims 2, 7-13, 15-17 and 19 patentably distinguish over the reference relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Conclusion

In accordance with the foregoing, claims 1, 2, 4 and 6-20 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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